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Digital Design Flow for Area-Constrained IPs Using Custom Non-standard IEEE-754 Format

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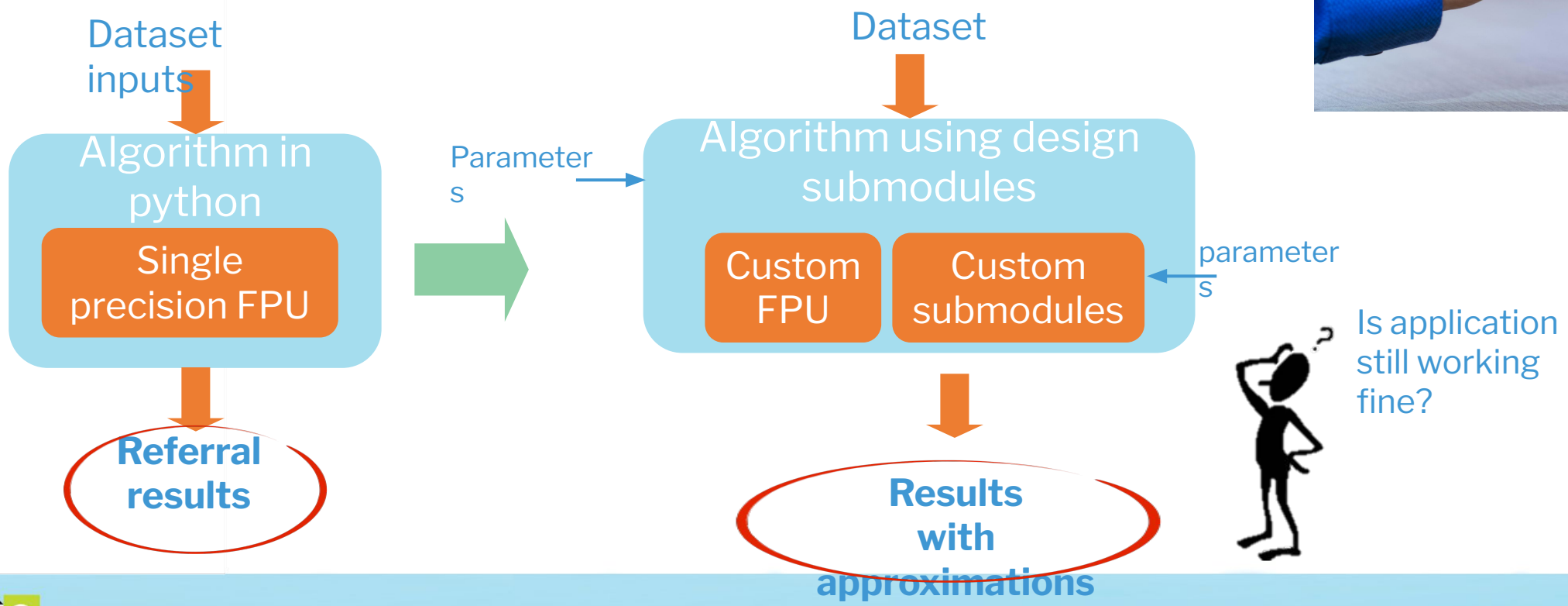
Motivation

Embedded digital algorithm in analog-on-top products

- Technology node is driven by analog specifications
- Data rate are limited (kHz range)
- Fast trade-offs study (accuracy, latency and area)

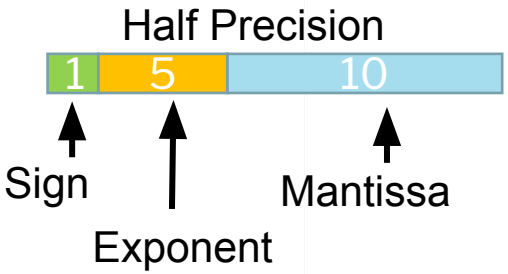
Main idea

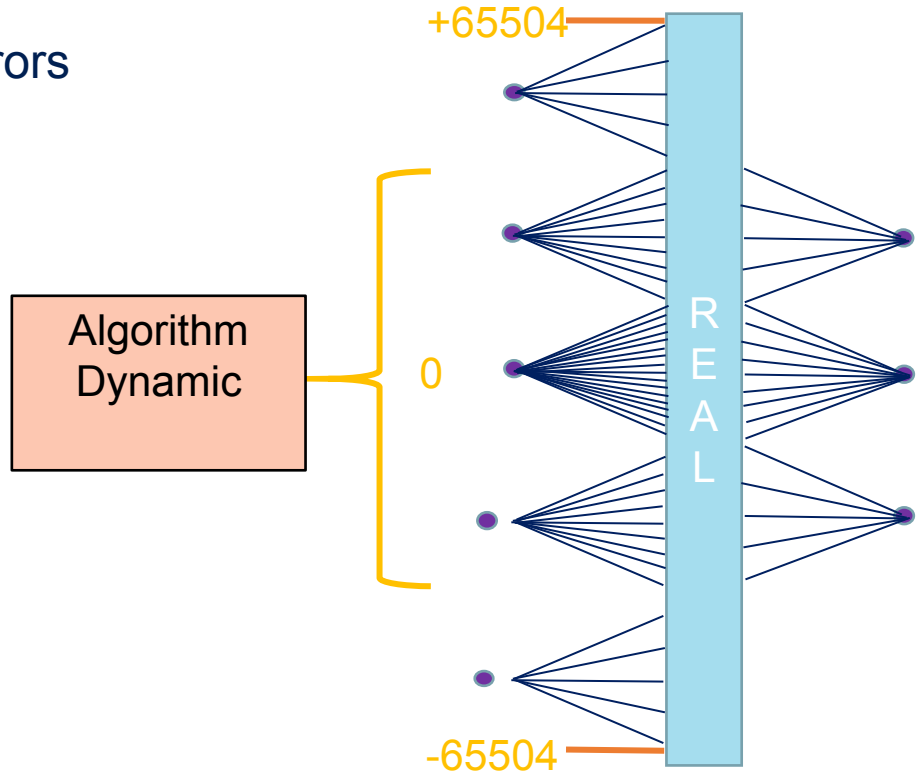
- Design exploration flow :
  - custom float point
  - custom parametric arithmetical submodules

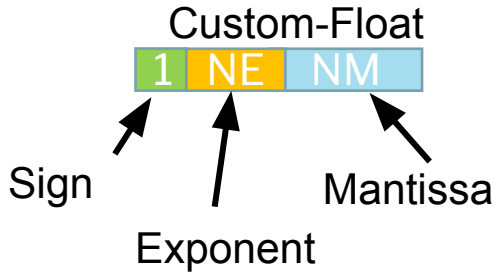


Custom floating point

- Real is simpler
- Accuracy at the output
- Float may be best area option
- Arithmetic library in float
- Technique to mitigate errors



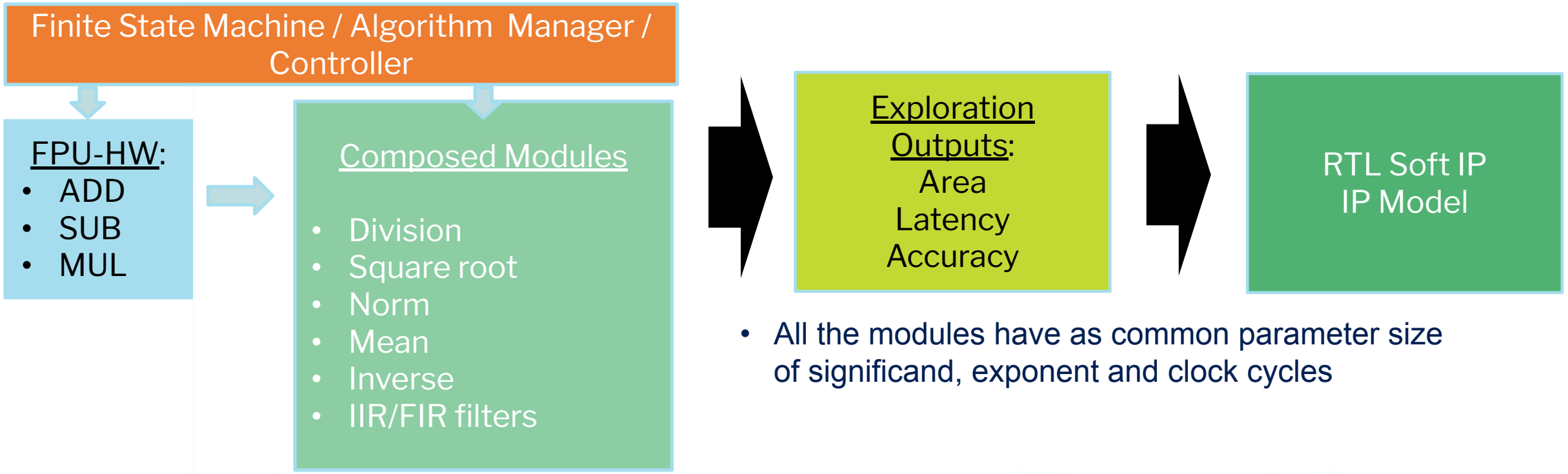




- Similar to IEEE754 → no NaN and no infinities
- Reduction of NE → dynamic reduction (underflow overflow)
- Reduction of NM → accuracy reduction

Additional content: non-standard IEEE 754 floating point arithmetical modules

- Basic configurable hardware modules
- Arithmetical submodules
- The automated flow generates trade-off reports
- RTL Soft IP and bit-true model



- All the modules have as common parameter size of significand, exponent and clock cycles

Evidence: step counter design example

From 16 to 8 bits custom float format -> 70% area reduction with a 0.4% accuracy loss

N Bit	NM	NE	Mean+2σ
16	10	5	10.31%
12	7	4	10.29%
10	6	3	10.33%
10	5	4	10.46%
8	4	3	10.71%

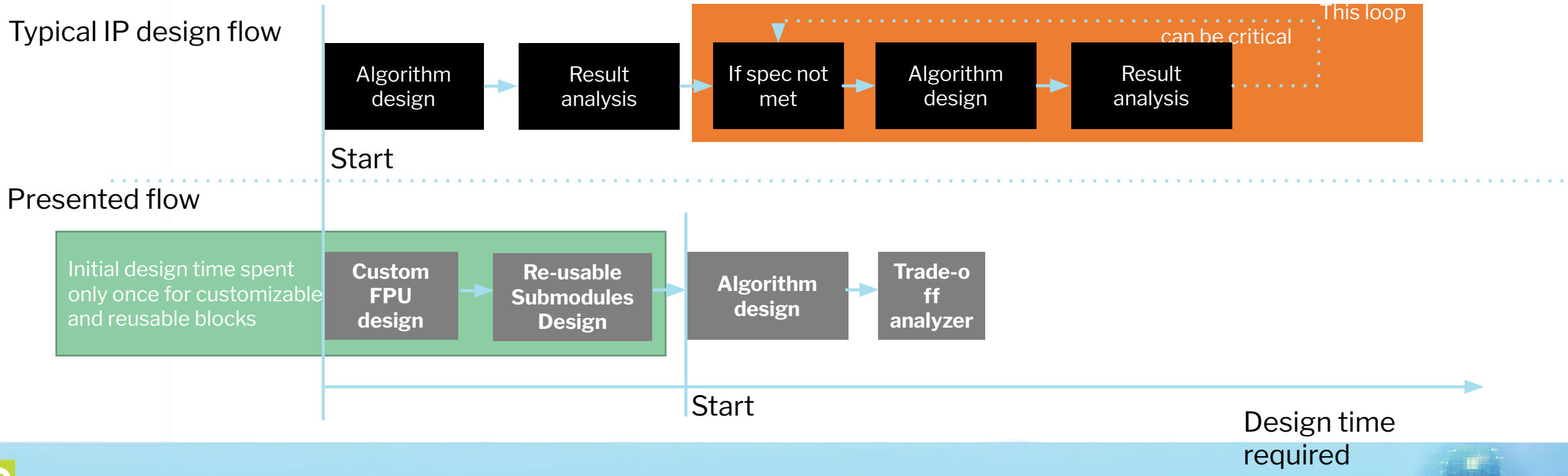
IEEE 754 Standard 16-bit arithmetic

	Area [μm^2]	%Reduction
M10E5	10447	-
M7E4	6336	39,3
M6E3	4343	58,4
M5E4	4407	57,8
M4E3	3126	70,1

Results are expressed as Mean+2σ of the percentual error between the computed number of steps vs the real number of steps

Summary – the digital design flow

- It tailors and matches the customer application needs appropriately
- It is very effective in area-constrained devices, where serialization design technique can be used for embedded complex algorithms
- It reduces the design time by decreasing the number of iterations to meet the specifications



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Thank You